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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,567	10/22/2001	Rebecca Yuan	15983US01	3737

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Christopher C. Winslade
McAndrews, Held & Malloy
500 W. Msdison Street, Suite 3400
Chicago, IL 60661

EXAMINER	
TRAN, KHANH C	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,567	YUAN, REBECCA	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-12 and 14-28* is/are rejected.

7)☒ Claim(s) *3,4 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 04/27/2006 has been entered. Claims 1-28 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see pages 10-14 of Applicant's Remarks, filed on 04/27/2006 has been entered, with respect to the rejection(s) of claim(s) 1-2 and 5-28 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Andren et al. U.S. Patent 5,654,991 (previously cited), Dutkiewicz et al. U.S. Patent 5,629,960 (previously cited), Giallorenzi et al. U.S. Patent 5,867,525 (previously cited) and Chen U.S. Patent 6,873,666 B2.

3. The objection of claim 4 has been withdrawn after Applicant amended claim to correct the informalities.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5-11 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andren et al. U.S. Patent 5,654,991 (previously cited) in view of Dutkiewicz et al. U.S. Patent 5,629,960 (previously cited) and Giallorenzi et al. U.S. Patent 5,867,525 (previously cited).

Regarding claim 1, in column 6 lines 15-50, figure 5 illustrates a bit sync clock adjustment circuit including an accumulator by position 42, a biggest selector 44, an adjacent sample comparator and bit sync adjust. The magnitude signal is provided to an accumulator 42 which sums the magnitudes associated with each sample position within a symbol.

In column 4 lines 25-35, Andren et al. expresses that in one aspect of the invention, the relationship among the early, largest and late samples can be used to adjust the bit synchronization with respect to the symbol timing of the received signal. Furthermore, in column 6 lines 15-48, with reference to FIG. 5, Andren et al. teaches a functional block diagram of a system, which could be used to adjust the bit synchronization may receive a signal, which provides a time series of magnitudes associated with each sample of a received signal. The magnitude signal may be provided to an accumulator 42 which sums the magnitudes associated with each sample position within a symbol. For example, the *accumulator may sum all the first samples (within each symbol) together, all the second samples together, etc. for a predetermined period of time.* The period of time over which the samples are

accumulated may be a function of the duration of the preamble or a portion of a preamble of the received signal.

Giallorenzi et al. teaches a portion of the receiver (shown in figure 2) includes accumulators 48 and 68 for averaging the on-time accumulated signal and the difference between the early despread signal and the late despread signal to reduce effects of noise.

Andren et al. and Giallorenzi et al. teachings are in the same field of endeavor. Andren et al. teaches the accumulator 42 which sums the magnitudes associated with each sample position within a symbol over a period of time. Because the accumulator as taught by Giallorenzi et al. averages the accumulated signal to reduce effects of noise, one of ordinary skill in the art at the time the invention was made would have been motivated to modify Andren et al. accumulator 42 to perform computation of the averaged sample sums of the early, largest and late sum samples.

In column 6 lines 15-48, Andren et al. teaches the accumulator sum all the first samples together, all the second samples together, etc. for a predetermined period of time. Upon the end of the selected period of time, the sums are evaluates by a biggest selector 44, which compares the accumulated sums and determines which set of samples contains the highest sum.

Andren et al. does not teach the samples are DC compensated samples as claim in the application claim.

Dutkiewicz et al. invention is directed to a method for reducing the effects of transients on the DC offset tracking stage and the symbol timing recovery stage. In

column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage tracks the mean DC offset and provides a DC offset voltage 32. DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. Because due to the variations in the digital information signal the DC off-set tracking stage and the symbol timing recovery stage lose synchronization with the system channel signal as discussed in Dutkiewicz et al. invention, it would have been obvious for one of ordinary skill in the art at the time of the invention that Andren et al. teachings can be modified to implement DC offset removal and DC tracking stage as taught in Dutkiewicz et al. invention. With the modification, accumulations of the early, on-time, and late sample sums account for the computed DC offset estimate.

Regarding Applicant's arguments on pages 12-13 in the Remark that Andren et al. teaches away the DC offset loop by minimizing additional circuitry and power consumption.

The Examiner's position is that Applicant's arguments are not persuasive. First, Andren et al. does not teach a DC offset loop because Andren et al. invention is directed to a method and apparatus fast acquisition bit timing loop. However, in column 1 line 60 via column 2 line 10, Dutkiewicz et al. recognizes that in the case in which transient interference occurs, signals received by the subscriber are distorted with large DC offset variations and amplitude variations. When these distorted received signals

are subsequently demodulated and A/D converted, the distortion manifests itself as variations in the mean DC offset and amplitude of the digital information signal (in the case of a non-coherent demodulator) and, in the case of a coherent demodulator, the transient distortion on the forward channel is seen as variations in the carrier frequency and the vector magnitude of the demodulated signal. Due to the variations in the digital information signal the DC off-set tracking stage and the symbol timing recovery stage lose synchronization with the system channel signal. Loss of synchronization results in degradation of the received signal or complete loss of the forward channel signal. Because the variations in the digital information signal the DC off-set tracking stage and the symbol timing recovery stage lose synchronization with the system channel signal, one of ordinary skill in the art would have been motivated to track the DC offset using DC tracking loop as taught in Dutkiewicz et al. invention.

Regarding claim 2, the biggest sum is positive when the sample sum is positive and is otherwise of a second value.

Regarding claims 5 and 6, as recited in claim 1, the accumulator sum all the first samples together, all the second samples together, etc. for a predetermined period of time. Hence, if the maximum sum is the third sample sum, the maximum sum and the adjacent samples are then passed to an adjacent sample comparator 46 which determines the extent to which the selected biggest set of samples are centered in the peak of the received signal and whether an adjustment in the bit sync clock is desirable.

Regarding claim 7, claim 7 is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 8, as recited in claim 7, with the modification, accumulation of the early sample sum accounts for the computed DC offset estimate. The early sample sum corresponds to the claimed first set of samples.

Regarding claim 9, Dutkiewicz et al. does not teach receiving a DC offset from an initial calculator. Nevertheless, one of ordinary skill in the art would have recognized that DC tracking stage 23 provides initial DC offset estimate to DC offset removal 22.

Regarding claim 10, Andren et al. and Dutkiewicz et al. do not teach the DC offset estimate using a pilot signal. In column 6 lines 15-50, because Andren et al. suggests the period of time over which the samples are accumulated may be a portion of a preamble of the received signal, it would have been obvious for one of ordinary skill in the art at the time of the invention that Andren et al. teachings can be modified to estimate DC offset using the preamble. As common knowledge of one of ordinary skill in the art, the pilot signal is inserted in the preamble.

Regarding claim 11, as recited in claim 1, the accumulator 42 accumulates sums of the early, on-time and late sample positions with respect to the symbol timing of the received signal. In view of that, the early, on-time and late sample positions can also be

used for DC offset compensation. Hence, the early sample positions are offset by one sample with respect to the on-time sample positions.

Regarding claim 19, claim 19 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 25, claim 25 is rejected on the same ground as for claim 10 because of similar scope.

5. Claims 12, 14-18 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen U.S. Patent 6,873,666 B2 in view of Dutkiewicz et al. U.S. Patent 5,629,960 (previously cited).

Regarding claim 12, in column 2 lines 20-45, Chen teaches in figure 2 a symbol timing recovery circuit including an accumulation module 53 (shown in FIG. 2) comprising a plurality of accumulator whose number the accumulation module includes accumulators whose number is equal to the number of the sampling points in a symbol. The accumulators receive the outputs of the selection circuit for accumulating phase differences of the same sampling points of continuous neighboring symbols. The comparison module is to compare the sums of phase differences outputted from the accumulators. The optimal sampling point corresponds to an accumulator having the smallest sum of the phase differences. In light of the foregoing disclosure, the comparison module performs an equivalent function of a maximum identifier.

Chen does not teach a DC offset compensator as set forth in the application claim.

Dutkiewicz et al. invention is directed to a method for reducing the effects of transients on the DC offset tracking stage and the symbol timing recovery stage. In column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a

symbol timing recover stage 25. The DC tracking stage tracks the mean DC offset and provides a DC offset voltage 32. DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. Because due to the variations in the digital information signal the DC off-set tracking stage and the symbol timing recovery stage lose synchronization with the system channel signal as discussed in Dutkiewicz et al. invention, it would have been obvious for one of ordinary skill in the art at the time of the invention that Chen teachings can be modified to implement DC offset removal and DC tracking stage as taught in Dutkiewicz et al. invention.

Regarding claim 14, referring to Dutkiewicz et al. invention, as recited in claim 12, in column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage 23 tracks the mean DC offset and provides a DC offset voltage 32 to the DC offset removal 22, which corresponds to the claimed DC offset compensator.

Regarding claim 15, Chen teachings are related digital wireless baseband demodulation. In light of the foregoing, one of ordinary skill in the art would have recognized that Chen receiver could be configured as a cellular phone.

Regarding claim 16, as appreciated by one of ordinary skill in the art, the cellular phone performs functions of a personal digital assistant, e.g. storing phone number,

scheduler, etc.. Furthermore, the recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997).*

Regarding claim 17, as recited in claim 15, Chen teachings are related digital wireless baseband demodulation. Because the receiver could be configured as part of a cellular device, the receiver can be considered as a peripheral device.

Regarding claim 18, as recited in claim 12, the accumulation module 53 (shown in FIG. 2) comprising a plurality of accumulator whose number the accumulation module includes accumulators whose number is equal to the number of the sampling points in a symbol. In light of the foregoing, one of ordinary skill in the art would have recognized that the accumulators include an on-time accumulator, an early accumulator and a late accumulator.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, the receiver in figure 1 of Dutkiewicz et al. invention shows an A/D converter 21, a DC tracking stage 23 connected to the A/D converter 21.

Regarding claim 27, a DC offset removal 22 is disposed intermediate the A/D converter 21 and the DC tracking stage 23. The DC offset removal 22 inherently performs initial estimation subtraction.

Regarding claim 28, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, with the combining teachings of Chen and Dutkiewicz et al., DC offset removal, taught by Dutkiewicz et al., plurality of accumulators taught and comparison module 54 taught by Chen constitute the claimed multi-hypothesis bit synchronizer.

Allowable Subject Matter

6. Claims 3-4 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanhcong Tran 07/05/2006
Primary Examiner KHANH TRAN